REMARKS

Reconsideration of the above referenced application in view of the following remarks is requested. Existing claims 1-33 remain in the application.

ARGUMENT

Claim Rejections – 35 USC § 112

Claims 11, 14, 18, 21, 24, and 28 are rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement.

The Examiner rejected these independent method claims for the reason that the phrase "inner relationship" was not described in the specification as to enable one of ordinary skill in the art to make and/or use the invention. In response filed on April 20, 2006, Applicant presented arguments that this rejection should be withdrawn. In response, the Examiner rejected Applicant's arguments for two reasons: (1) evidence provided by Applicant is not sufficient to overcome the rejection for lack of enablement under 35 USC 112, first paragraph; (2) evidence to supplement a specification which on its face appears deficient under 35 USC § 112 must establish that the information which must be read into the specification to make it complete would have been known to those of ordinary skill in the art.

Here Applicant respectfully disagrees. First, the evidence provided by Applicant is sufficient to overcome the rejection for lack of enablement under 35 USC § 112, first paragraph. The specification (see e.g., paragraph [0014] of the specification) along with the claim language in the initial disclosure makes the disclosure enabling for the

limitation "inner relationship." The Examiner's main point is: were the description that an "inner cache" is referred to as an L1 cache and "outer cache" as an L2 cache considered as enabling for "inner relationship," the limitation "inner relationship" would be equivalent to "L1 relationship." Applicant respectfully disagrees with this argument presented by the Examiner. It is common known that caches are classified as L1, L2, or L3 based on their closeness to the processor. L1 cache is built into the processor and thus is normally referred to as "inner cache;" while L2 is normally external to a processor and thus is normally referred to as "outer cache." For reference only, the Examiner may look "L1 cache" or "L2 cache" in any technical dictionary (e.g., http://www.webopedia.com/"). Based on this fact, the "inner relationship" is relative to a processor. When claims 11, 14, 18, 21, 24, and 28 use the term "inner relationship," it implies that the first cache is closer to the processor than the second cache. Thus, the limitation "inner relationship" can be reasonably inferred from the specification and the evidence from the specification is sufficient to overcome the rejection for lack of enablement under 35 USC § 112, first paragraph.

Second, the evidence to supplement the specification (i.e., L1 cache is closer to the processor than L2 cache) is known to those of ordinary skill in the art as evidenced by the definition of L1 or L2 cache in a technical dictionary (e.g., http://www.webopedia.com/).

For the forgoing, Applicant strongly believe that the initial disclosure is enabling for the limitation "inner relationship" recited in claims 11, 14, 18, 21, 24, and 28. Thus, Applicant respectfully requests that the Examiner reconsider Applicant's arguments and withdraw this rejection under 35 USC § 112, first paragraph.

Claim Rejections – 35 USC § 103

Claims 1 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli (6,629,268) (hereinafter Arimilli_1) in view of WO 00/52582 (hereinafter WO reference).

Claims 2-10 and 32-33 are rejected under 35 U.S. C. 103(a) as being unpatentable over Arimilli_1 in view of the WO reference and further in view of Arimilli (2002/0129211) (hereinafter Arimilli_2).

To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. MPEP § 706.02(j). Here the Examiner failed to establish a prima facie case of obviousness because at least the combination of Arimilli_1 and the WO reference does not teach or suggest all the claim limitations. For example, the combination of Arimilli_1 and the WO reference does not teach or suggest a cache containing a cache line with a first cache coherency state when accessed from said first interface and a second cache coherency state when accessed from said second interface. In the Final Office Action issued on July 19, 2006, the Examiner asserted that the WO reference discloses this limitation. Applicant respectfully disagrees.

The Examiner specifically cited Fig. 1; page 11, lines 16-32; and page 12, lines 21-27 of the WO reference as disclosing the above-mentioned limitation. A careful

review of the cited portion of the WO reference reveals that they do not disclose the claimed limitations. Although Fig. 1 of the WO reference shows that two coherency states may be associated with a cache line. However, the cited portion of the WO reference does not disclose that a first cache coherency state is associated with accesses from the first interface and a second cache coherency state is associated with accesses from the second interface. In fact the cited portions of the WO reference do not disclose how the two coherency state method as shown in Fig. 1 works. Because the cited portions of the WO reference do not teach or suggest the claimed limitation as recited in independent claims 1 and 31, the Examiner has not established a prima facie case of obviousness under 35 USC § 103. Thus, Applicant respectfully requests that the 35 USC § 103 rejections of independent claims 1 and 31 over Arimilli_1 in view of the WO reference be withdrawn.

Because independent claims 1 and 31 are now patentable over Arimilli_1 in view of the WO reference, all of the claims that depend therefrom (i.e., claims 2-10 and claims 32-33, respectively) are also patentable over the combination of Arimilli_1 and the WO reference.

Claims 11-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli_2 in view of the WO reference.

Regarding independent claims 11, 14, 18, 21, 24, and 28, the Examiner asserted that Fig. 3, page 7; line 27 to page 8, line 13; and page 15, lines 1-19 of the WO reference discloses the limitation of transitioning a first cache coherency state to a joint cache coherency state including a first cache coherency state for outer interfaces and a

third cache coherency state for inner interfaces. Applicant respectfully disagrees. Fig. 2 of the WO references shows a state transition diagram based on MESI protocol and Fig. 3 of the WO reference shows the state transition diagram based on the MESI protocol with expanded coherency states (i.e., joint states). There is no showing by the cited portions of the WO reference of transitions from a single MESI coherency state (e.g., M or E) to a joint coherency state (e.g., MI), as recited by the claimed limitation.

Additionally, there is no showing by Fig. 3 or page 15, lines 15-19 of the WO reference of the limitation of transitioning the second cache coherency state to the third cache coherency state. Fig. 3 only shows transitions between joint cache states (e.g., EM, MI, ES, etc.). Page 15, lines 15-19 of the WO reference provides, "The state MS occurs when an SLC reads Shared. As already noted several times above, however, an SLC may cause a logically reduced state after a corresponding action, so that finally one of the states I or S may be behind the state description MS for an affected SLC." Applicant cannot find explicitly or implicitly that the quoted portion of the WO reference discloses the limitation of transitioning the second cache coherency state to the third cache coherency state.

For the foregoing reasons, the combination of Arimilli_2 and the WO reference does not teach or suggest all of the limitations recited in independent claims 11, 14, 18, 21, 24, and 28. Thus, these claims are patentable over Arimilli_2 in view of the WO reference. Accordingly, all of the claims that depend therefrom are also patentable over Arimilli_2 in view of the WO reference. Applicant hereby respectfully requests that the Examiner withdraw the 35 USC § 103 rejections of claims 11-30 and reconsider the application.

CONCLUSION

In view of the foregoing, existing claims 1-33 are all in condition for allowance. If the Examiner has any questions, the Examiner is invited to contact the undersigned at (503) 264-1700. Early issuance of a Notice of Allowance is respectfully requested.

Respectfully submitted,

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